CIRCUITRY FOR MITIGATING PERFORMANCE LOSS ASSOCIATED WITH FEEDBACK LOOP DELAY IN DECISION FEEDBACK EQUALIZER AND METHOD THEREFOR

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to a decision feedback equalizer (DFE). More specifically, the present invention relates to circuitry for mitigating the performance loss caused by the feedback loop delay in a DFE. A corresponding method is also disclosed.

2. Discussion of Related Art

A digital transmission is susceptible to multipath fading or the like and invites waveform distortion of the transmitted signal resulting in degradation of signal quality. In order to minimize this problem, it is the current practice to employ an automatic adaptive equalizer using a transversal filter. An adaptive equalizer may be classified into linear and non-linear types. Linear equalization has found extensive use in terrestrial digital microwave communications systems. However, it is unable to effectively minimize deep or severe multipath distortion. Therefore, residual intersymbol interference undesirably increases. In particular, as a signal transmission rate becomes higher and signal propagation distance increases, the linear equalization is no longer sufficient to handle severe frequency selective fading wherein multipath delay spreads over a transmission symbol period. To overcome this problem, a non-linear type equalizer, which takes the form of a decision feedback equalizer (DFE), is often employed. In other words, DFEs are commonly utilized in digital communication systems to reduce the multi-path impairments caused by the channel.

The ATSC standard set forth by the Advanced Television Systems Committee in the document entitled "ATSC Digital Television Standard" (Document A53, September 16, 1995), for terrestrial Digital TV in the United States requires transmission of an MPEG bit stream of 19.28 Mbps over a bandwidth of 6 MHz at a symbol rate of 10.76 MHz in the VHF and UHF carrier frequency range. The modulation scheme used is a single carrier 8 level Vestigial Sideband (VSB) modulation scheme. Systems such as the North American Terrestrial Digital TV rely on DFEs to reduce the multipath impairments.

U.S. Patent No. 5,119,401 to Tsujimoto discloses a decision feedback equalizer including forward part whose signal reference point is shiftable depending on channel response. In the '401 patent, Fig. 1 depicts a non-linear type equalizer in the form of a decision feedback equalizer (DFE) denoted by reference numeral 30. The DFE includes a forward equalizer (FE) 32 and a backward equalizer (BE) 34. A center tap c_O of the overall DFE 30 is positioned at the final tap of the forward equalizer as shown. The forward equalizer 30 includes N-1 delay circuits 36 coupled in series, N multipliers 38, and an adder 40. On the other hand, the backward equalizer 34 is provided with M delay circuits 42, M multipliers 44 and an adder 46. Further, the DFE 30 includes a decision circuit 48, two subtractors 50, 52, and a tap control signal generator 54.

The DFE 30 operates to minimize intersymbol interference (ISI) in any received signal due to a precursor of an impulse response at the forward equalizer 32, while minimizing ISI caused by a postcursor at the backward equalizer 34. The output of the forward equalizer 32 is subtracted from the output of the backward equalizer 34 at the subtractor 50. The decision signal a_n (output by the decision circuit 48 and then fed back to the backward equalizer 34) is free of intersymbol interference and noises. Therefore, the equalization capability of the backward equalizer 34 using the decision feedback technique is higher than that of the forward equalizer 32. This means that the backward equalizer 34 is capable of completely removing ISI caused by a postcursor of impulse response (viz., minimum phase shift fading). It is understood that the DFE 30 is superior to the case where only the forward equalizer 32 is provided.

On the other hand, intersymbol interference due to a precursor (non-minimum phase shift fading) is equalized at the forward equalizer 32. Consequently, in connection with the ISI due to non-minimum phase shift fading, the DFE 30 merely implements equalization which is identical to that of the forward equalizer 32. This is the reason why a easily installed linear equalizer 32 is chiefly employed rather than a complex DFE in terrestrial digital microwave communications systems, permitting severe distortion due to non-minimum phase fading to occur frequently.

A known approach to effectively removing intersymbol interference caused by non-minimum phase shift fading, is to provide a matched filter (MF) which is followed by a decision feedback equalizer (DEF). Fig. 2 is a block diagram showing one example of this MF/DEF arrangement. The decision feedback equalizer (DFE) 30, which is identical to the arrangement illustrated in Fig. 1, is preceded by a matched filter 60 which includes a plurality of delay circuits 62, each having a symbol interval T/2, a plurality of multiplexers 64, and a tap control signal generator 68. As is well known, a matched filter maximizes the output ratio of peak signal power to mean noise power. The MF/DFE arrangement exhibits excellent precursor distortion equalization performance as compared with the case where the DFE only is provided. However, the MF/DFE is inferior to the DFE in connection with the equalization of the postcursor distortion. This problem, inherent in the MF/DFE, is caused by new waveform distortion introduced by the provision of the MF 60.

U.S. Patent No. 5,119, 401 proposes to improve the performance of the decision feedback equalizer by providing a DFE having a forward equalizer whose center tap is shifted by at least one symbol interval towards the final stage of the equalizer. As shown in Fig. 3, the DFE 100 differs from that shown in Fig. 1 in that the DFE of Fig. 1 has be modified to include two subtractors 102, 104, two correlators 106, 108, and a tap control signal generator 110; moreover, the center tap c_0 of the former arrangement is one-tap shifted towards the input thereof and hence the last tap is denoted by c+1.

It will be appreciated that conventional DFEs, such as thus discussed above, require very long taps in both its forward (FE) and feedback (FBE) equalizers, e.g., impulse filters, to combat the multipath impairment attributable to the channel. Due to design constraints, such long filters are often realized using pipeline structures. Such pipeline structures often introduce unwanted delay, i.e., implementation delay. Moreover, it will be noted that the delay in the feedback path of the equalizer results in a performance penalty. The performance of the equalizer will be degraded for those postcursor echoes that are very close to the main path. For such echoes, little help is provided by the feedback filter, stressing the forward equalizer to do most of the equalization.

Since postcursor echoes close to the main path are common in terrestrial channels, it would be extremely desirable if the feedback path could be realized without unwanted delay. Thus, what is need is a method and corresponding circuitry for mitigating the performance loss associated with feedback loop delay in a DFE. It would be beneficial if the thus improved method and corresponding DFE circuitry could be implement at little or no additional cost.

SUMMARY OF THE INVENTION

Based on the above and foregoing, it can be appreciated that there presently exists a need in the art for a method and corresponding circuitry which mitigates performance loss caused by feedback loop delay in a decision feedback equalizer which overcomes the above-described deficiencies. The present invention was motivated by a desire to overcome the drawbacks and shortcomings of the presently available technology, and thereby fulfill this need in the art.

According to one aspect, the present invention provides a first and second Feedback Equalizer signals for controlling a decision feedback equalizer, wherein the first Feedback Equalizer signal is delayed by an implementation delay and wherein the second Feedback Equalizer signal is free of the implementation delay.

According to another aspect, the present invention provides a decision feedback equalizer (DFE) including a forward equalizer, first and second adders, a decision device, a Feedback Equalizer, and an N-tap filter. Preferably, the first and second adders, the decision device, and the Feedback Equalizer constitute a first feedback loop, the second adder, the decision device, and the N-tap filter constitute a second feedback loop. In that case, the second feedback loop is free of an implementation delay associated with the first feedback loop. In the exemplary DFE, N is a positive integer. If desired, the N-tap filter is implemented in fast logic.

According to a further aspect, the present invention provides a digital television receiver including the DFE as recited immediately above.

According to a still further aspect, the present invention provides a decision feedback equalizer (DFE), including a forward equalizer, a decision device, circuitry for generating a first feedback signal responsive to first filter coefficients adapted to process postcursor echoes adjacent to the main channel and a second feedback signal responsive to second filter coefficients adapted to process all other postcursor echoes, and circuitry for applying the first and second feedback signals to thereby control the DFE. In an exemplary case, the number of second filter coefficients is much greater than the number of first filter coefficients.

According to a further aspect, the present invention provides a method for controlling a decision feedback equalizer (DFE) including a forward equalizer and a decision device. Preferably, the method includes steps for generating a first feedback signal responsive to first filter coefficients adapted to process postcursor echoes adjacent to the main channel, generating a second feedback signal responsive to second filter coefficients adapted to process all other postcursor echoes, and applying the first and second feedback signals to thereby control the DFE. In an exemplary case wherein the decision device is common to first and second feedback loops, the applying step can include steps for applying the first and second feedback signals to the first and second feedback loops, respectively, to thereby control the DFE.

BRIEF DESCRIPTION OF THE DRAWINGS

These and various other features and aspects of the present invention will be readily understood with reference to the following detailed description taken in conjunction with the accompanying drawings, in which like or similar numbers are used throughout, and in which:

Fig. 1 is a block diagram illustrating a conventional decision feedback equalizing arrangement including a forward equalizer and a backward equalizer;

Fig. 2 is a block diagram illustrating a conventional equalizing arrangement which includes a matched filter in the upstream signal flow path of the decision feedback equalizing arrangement shown in Fig. 1;

Fig. 3 is a block diagram illustrating another conventional decision feedback equalizing arrangement having a shifted center tap;

Fig. 4 is a high-level block diagram of a preferred embodiment of a decision feedback equalizer implemented in a digital television (DTV) receiver according to the present invention;

Fig. 5 is a high-level block diagram of another preferred embodiment of the decision feedback equalizer implemented in a digital television (DTV) receiver according to the present invention; and

Fig. 6 depicts a family of curves illustrating the performance improvement of the DFE according to Fig. 4 with a conventional DFE.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the discussion which follows, the decision feedback equalizer (DFE) under discussion advantageously can be implemented in a digital television (DTV) receiver or the like. However, it will be appreciated that the improved DFE can be employed in a myriad of digital receivers.

Fig. 4 illustrates a first preferred embodiment of a decision feedback equalizer 200 according to the present invention, which includes a forward equalizer 210 connected to a first input port of a first adder 220, a second adder 230 coupled to the output port of the first adder 220. The output port of the second adder 230 is connected to a decision device 240, the output of which is connected to both the input port of a feedback equalizer 250 and the input port of an N tap filter 260. Preferably, the output of the feedback equalizer 250 is provided to a second input port of the first adder 220 while the output of the N-tap filter 260 is provided to a second input port of the second adder 230.

Fig. 5 illustrates a second preferred embodiment of a decision feedback equalizer 200' according to the present invention, which includes a forward equalizer 210' connected to a first input port of a first adder 220', a second adder 230' coupled to the second input port of the first adder 220'. The output port of the first adder 220' is connected to a decision device 240', the output of which is connected to both the input port of a feedback equalizer 250' and the input port of an N tap filter 260'. Preferably, the outputs of both the feedback equalizer 250' the N-tap filter 260' are provided to the respective input ports of the second adder 230'.

By comparing the DFE 200 illustrated in Fig. 4 and the DFE 200' depicted in Fig. 5 with the DFE 30 illustrated in Fig. 1, it will be appreciated that the preferred embodiments according to the present invention include a small delay compensation filter, i.e., an N-tap filter, in parallel with the feedback equalizer 250, 250.' It will be also appreciated that both of the feedback equalizers 250, 250' can be implemented as finite impulse response (FIR) filters similar to those depicted in Figs. 1-3.

It should be noted that the length of the N-tap filters 260, 260' equal the number of the unwanted symbol delay, i.e., the implementation delay, introduced by the feedback equalizer loop. For example, when all the implementation delay associated with the feedback equalizer loop are completed within three (N + 1) symbols, then the length of the N-tap filter will be two taps.

The operation of the improved decision feedback equalizer according to the present invention can perhaps best be understood by conceptualizing the feedback equalizer as being a single FIR filter with 100 taps to which coefficients C1 to C100, respectively, are applied that is implemented in two stages. In other words, with respect to Fig. 4, the feedback equalizer includes a first stage feedback equalizer (equalizer 250) implementing coefficients C3 to C100 and a second stage feedback equalizer (N-tap filer 260) implementing coefficients C1 to C2. Preferably, the N-tap filter 260 is implemented in fast logic so as to minimize implementation delays. Thus, decision feedback equalizer 200 includes a first loop defined by feedback equalizer 250 and a second loop defined by the N-tap filter 260. Advantageously, the coefficients implemented in the N-tap filter 260 can be selected to optimize the processing of postcursor echoes that are very close to the main path.

The loop closed by the N-tap filter 260 can be completed within one symbol period, i.e., within the minimum delay needed (including tap adaptation). Algorithmically, the overall unwanted delay in the feedback path is removed while the design constraints on the feedback equalizer 250 is still relaxed to permit modest pipeline stages.

It should be mentioned that the decision feedback equalizer 200' illustrated in Fig. 5 introduces an additional implementation delay due to the second adder 230' disposed between the output of the feedback equalizer 250' and the first adder 220'. This implementation delay cannot be mitigated by modification of the N-tap filter 260', e.g., implementing an N+1- or N-1-tap filter in place of the N-tap filter depicted in Fig. 5. However, when the decision feedback equalizer according to the present invention is implemented, for example, as a combination of software controlling a digital signal processor, the implementation delay may be considered insignificant.

To illustrate the advantages of the decision feedback equalizers 200, 200' illustrated in Figs. 4 and 5, computer simulations were performed utilizing a channel with impulse response

(1.0, 0.8). Fig. 6 plots the simulation result in terms of signal-to-noise ratio (SNR) versus symbol error rate (SER) for the circuits illustrated in Figs 1 and 4. As shown in Fig. 6, the method according to the present invention provides more than 1.5dB performance improvement compared to the practical equalizer with a delay in its feedback path.

It should be mentioned that there are other advantages to the decision feedback equalizer (DFE) illustrated in Fig. 4 than the static performance advantage. For example, the decision feedback equalizer 200 exhibits faster convergence and better tracking of dynamic channels that contains significant postcursor echoes next to the main path.

For a given technology, a straight forward technique for removing the unwanted latency is to design the feedback part using special adder and multiplier structures in place of the N-tap filter discussed above. This substitution of elements would be particularly advantageous for filters with a relatively small number of taps, but could prove to be inadequate for filters with a relatively large number of taps. At the same time, it will also be noted that the inclusion of additional elements such as the above-mentioned adders and multipliers would increase the design time for the DFE.

It should be mentioned that while the discussion of the preferred embodiments addressed applications involving DTV receivers, the invention is not limited to such applications. Thus, although presently preferred embodiments of the present invention have been described in detail herein, it should be clearly understood that many variations and/or modifications of the basic inventive concepts herein taught, which may appear to those skilled in the pertinent art, will still fall within the spirit and scope of the present invention, as defined in the appended claims.